GENERAL DESCRIPTION

Model 990/10A Computer

Part No. 2302633-9701 *A
February 1984

TEXAS INSTRUMENTS

Preface

This manual provides information about the Model 990/10A Computer and is directed to both the installation personnel and the end-user.

Information in this manual is divided into the following sections:

Section

1 General — Contains physical and functional descriptions that acquaint the user with the hardware components and capabilities of the Model 990/10A Computer.

2 Installation — Outlines procedures for unpacking the Model 990/10A Computer from its shipping container and setting the option jumpers and switches.

3 Operation — Describes the indicators on the front panel and PWB and provides general operating procedures.

4 Programming — Presents information for use by programmers on the function of the processor and the asynchronous communication controller.

Appendix

A Using the Multiprocessing Interface — Contains information on system configuration and programming the multiprocessing interface.

The following documents contain additional information related to the Model 990/10A Computer.

Title	Part Number
Model 990/10A Computer Maintenance Manual — Field Theory and Maintenance	2302634-9701
Model 990/10A Computer Maintenance Manual — Depot Theory and Maintenance	2302635-9701
Model 990 Computer 990/10 and 990/12 Assembly Language Reference Manual	2270509-9701
Model 990 Computer Diagnostics Handbook	945400-9701
Model 990A13 Chassis Maintenance Manual — General Description	2308774-9701
ROM Loader User's Guide	2270534-9701

1.5.7 Backpanel Interface

All connections to the computer chassis and peripheral devices (other than the front panel and EIA port) are through the backpanel connector. Table 1-5 and Table 1-6 list the pins and definitions for the backpanel connector.

Table 1-5. Backpanel Connector P1

Pin Number	Slot 1 Signal	In/Out	Not Slot 1 Signal	In/Out	Comments
1, 2	GND	—	GND	—	
3, 4	+5 MAIN	I	+5 MAIN	I	
5, 6	NO CONNECT	—	NO CONNECT	—	(+12V MEMORY)
7, 8	+5 MEMORY	I	+5 MEMORY	I	MAIN AFTER SLOT 7
9, 10	NO CONNECT	—	NO CONNECT	—	(-5V MEMORY)
11	TLREAD	I/O	TLREAD	I/O	
12	GND	—	GND	—	
13	TLPRES-	I	TLPRES-	I	
14	TLIORES-	O	TLIORES-	I	470 OHM PULL-UP IN SLOT 1
15	GND	—	GND	—	
16	TLPFWP-	I	TLPFWP-	I	
17	GND	—	GND	—	
18	CRUBITOUT	O	OPEN(CRUBITOUT)*	—	
19	GND	—	GND	—	
20	TLTM-	I/O	TLTM-	I/O	
21	GND	—	GND	—	
22	STORECLK-	O	OPEN(STORECLK-)*	—	
23	MODSEL0-	O	OPEN*	—	
24	GND	—	GND	—	
25	TLGO-	I/O	TLGO-	I/O	
26	GND	—	GND	—	
27	TLDAT12-	I/O	TLDAT12-	I/O	
28	TLDAT13-	I/O	TLDAT13-	I/O	
29	120HZ	I	120HZ	I	
30	TLDAT14-	I/O	TLDAT14-	I/O	
31	TLDAT15-	I/O	TLDAT15-	I/O	
32	CRUBIT13	O	OPEN(CRUBIT13)*	—	
33	NO CONNECT	—	NO CONNECT	—	IAQ- ON /10
34	CRUBIT15	O	OPEN(CRUBIT15)*	—	
35	MODSEL1-	O	OPEN*	—	
36	CRUBIT12	O	OPEN(CRUBIT12)*	—	
37	MODSEL2-	O	OPEN*	—	
38	CRUBIT14	O	OPEN(CRUBIT14)*	—	
39, 40	NO CONNECT	—	NO CONNECT	—	(+12V MAIN)
41, 42	NO CONNECT	—	NO CONNECT	—	(-12V MAIN)
43	MODSEL3-	O	OPEN*	—	
44	MODSEL4-	O	OPEN*	—	
45	MODSEL5-	O	OPEN*	—	
46	MODSEL6-	O	OPEN*	—	
47	MODSEL7-	O	OPEN*	—	

Table 1-5. Backpanel Connector P1 (Continued)

Pin Number	Slot 1 Signal	In/Out	Not Slot 1 Signal	In/Out	Comments
48	MODSEL8-	O	OPEN(MODSELB-)*	—	
49	MODSEL9-	O	OPEN*	—	CBDAT(0)—
50	CRUBIT7	O	OPEN(CRUBIT7)*	—	
51	MODSEL10-	O	OPEN*	—	CBDAT(1)—
52	CRUBIT6	O	OPEN(CRUBIT6)*	—	
53	MODSEL11-	O	OPEN*	—	CBDAT(2)—
54	CRUBIT5	O	OPEN(CRUBIT5)*	—	
55	TLMER-	I/O	TLMER-	I/O	
56	CRUBIT4	O	OPEN(CRUBIT4)*	—	
57	GND	—	GND	—	
58	TLAV	I	TLAV	I	
59	GND	—	GND	—	
60	CRUBITIN	I	CRUBITIN	—	470 OHM PULL-UP IN SLOT 1
61	MODSEL12-	O	OPEN*	—	CBDAT(3)-
62	CRUBIT8	O	OPEN(CRUBIT8)*	—	
63	TLWAIT-	I	TLWAIT-	I	
64	CRUBIT9	O	OPEN(CRUBIT9)*	—	
65	NO CONNECT	—	NO CONNECT	—	
66	INTP1A-	O	INTP1A-	O	HOST INTERRUPT
67	MODSEL13-	O	OPEN*	—	CBDAT(4)-
68	CRUBIT10	O	OPEN(CRUBIT10)*	—	
69	MODSEL14-	O	OPEN*	—	CBDAT(5)-
70	CRUBIT11	O	OPEN(CRUBIT11)*	—	
71	TLAK-	I/O	TLAK-	I/O	
72	GND	—	GND	—	
73	NO CONNECT	—	NO CONNECT	—	TLCACHEN ON /12
74	CBTEST	—	CBTEST	—	GND IN CHASSIS
75	NO CONNECT	—	NO CONNECT	—	
76	MODSEL15-	O	OPEN*	—	
77, 78	+5 MAIN	I	+5 MAIN	I	
79 ,80	GND	—	GND	—	

Note:

* Outputs tristate, inputs disabled by slot 1 switch.

2.3 990/10A INSTALLATION PROCEDURES

The following paragraphs describe the preparation and installation of the 990/10A computer board.

WARNING

Ensure that the chassis ac power cord is disconnected from power while performing the installation procedures. Failure to observe this precaution could result in severe electrical shock.

2.3.1 Setting Option Switches and Jumpers on the 990/10A Board

Two dual in-line pack (DIP) switches and five jumpers are provided on the 990/10A board for option setting. Figure 2-1 shows the locations of these switches and jumpers. Figure 2-2 shows the locations of these switches and jumpers on the 1-megabyte processor board.

The eight-position switch contains the slot 1 switch in the leftmost position (SW1) and sets the address of the memory error log in the remaining seven positions (SW2 through SW8). The slot 1 switch disables certain slot 1 functions for operating the 990/10A as an auxiliary processor and should be off for normal slot 1 operation. Table 2-1 describes setting the memory control switches.

The four-position DIP switch controls the lower bound address of the on-board memory and is set simply by coding in the binary equivalent of the most significant hexadecimal digit of the desired beginning TILINE address (see Table 2-2). For a typical single processor system, all switches should be off.

Table 2-1. Memory Control TPCS Addresses

Logical Address (Hexadecimal)	Physical Address (Hexadecimal)	SW2	SW3	SW4	SW5	SW6	SW7	SW8
F800-06	FFC00-03	Off	Off	Off	Off	Off	Off	Off
F808-0E	FFC04-07	Off	Off	Off	Off	Off	Off	On
FB00-06[1]	FFD80-83	On	On	Off	Off	Off	Off	Off
:	:	:	:	:	:	:	:	:
FBF0-F6	FFDF8-FB	On	On	On	On	On	On	Off
FBF8-FE[2]	FFDFC-FF	On	On	On	On	On	On	On

Notes:

Memory size jumpers do *not* exist on the 1-megabyte processor board.

[1] Suggested default.

[2] This setting causes self-test to fail with a front panel code of >0030.

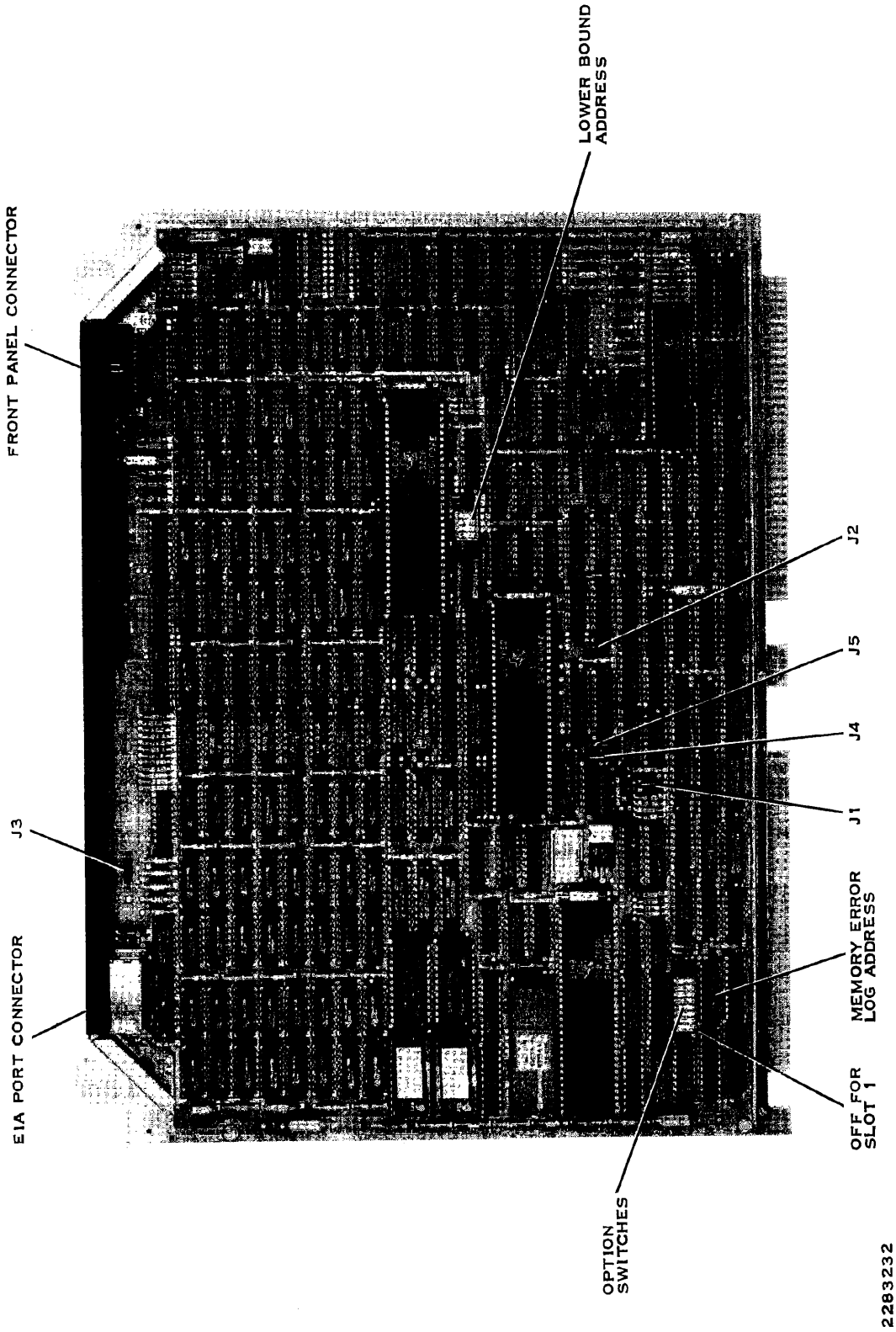

Figure 2-1. Switch and Jumper Locations

The five jumpers on the 990/10A are listed in Table 2-3. When installed, jumper J1 causes the EIA port interrupt to be "OR"ed with any backpanel interrupt connected to interrupt level 8. Jumper J2 is a two-position jumper that allows the user to select whether the real-time clock interrupts at interrupt level 5 or 15. For typical applications, the jumper should be installed in the level 5 position. If the jumper is removed, there will be no real-time clock interrupt. Jumper J3 allows the user to select whether data set ready or data carrier detect is used to determine the ready condition of the EIA device. Data set ready should be used for typical applications. Jumper J4 should be removed if the user desires the processor to perform a load on every power up. Jumper J5 should be removed to use the 990/10A as an auxiliary processor. Each of these functions is explained in more detail in Section 1 of this manual.

Table 2-2. 990/10A Starting Address Switch Settings

Beginning Byte Address on Board	SW1	SW2	SW3	SW4	Number of Memory Bytes Below Board
>020000	Off	Off	Off	On	131,072
>040000	Off	Off	On	Off	262,144
>080000	Off	On	Off	Off	524,288
>0C0000	Off	On	On	Off	786,432
>100000	On	Off	Off	Off	1,048,576
>140000	On	Off	On	Off	1,310,720
>180000	On	On	Off	Off	1,572,864
>1C0000	On	On	On	Off	1,835,008

Table 2-3. Option Jumpers

Jumper	Pin 1 Location	Signature	Function
J1	BD053	PRT1INT-	EIA port interrupt
J2	CE074	RTCINT-	Real-time clock interrupt
J3	KF039	DSRA	Data set ready source
J4	CB057	PULOAD-	Load on power-Up
J5	CB059	HOST-	HOST/AUX jumper

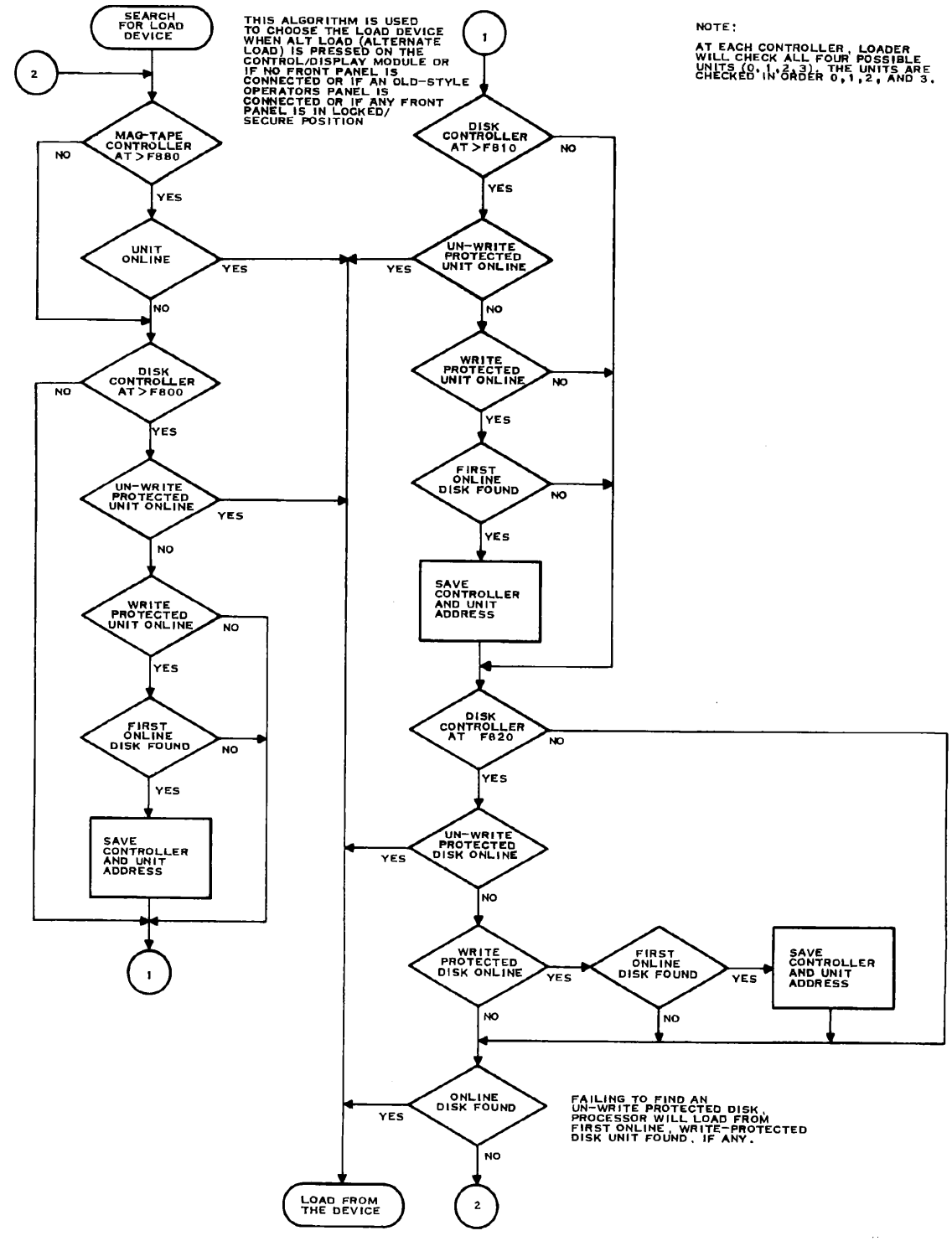

Figure 3-2. Universal Loader Search Algorithm

3.3 990/10A PWB INDICATORS

On the top edge of the 990/10A printed wiring board (PWB), there are additional LED indicators that can be seen by looking into the chassis interior. Figure 3-3 shows an edge view of the 990/10A board and the LED indicators. These indicators are explained in the following paragraphs.

3.3.1 Major Fault LED

The MAJFAULT LED indicator is illuminated on power-up and extinguished after the kernel test portion of self-test shows that no major fault exists within the microprocessor-ROM core of the board. Unless the major fault logic itself fails, MAJFAULT should always be illuminated when power is initially applied to the board. If this LED fails to extinguish, the processor may have a failure that prohibits displaying other error indicators.

3.3.2 FAULT LED

The FAULT LED indicator is a duplicate of the FAULT indication on the CDM. It is software-controlled to show a self-test, loader, or operating system fault.

3.3.3 Memory Error Indicators

The remaining LEDs on the 990/10A PWB provide the service person with indications of a failed memory component. This information is also available to software through the memory error log and will not generally require the user's attention.

3.3.3.1 Double-Bit Error. The MER LED indicator designates the occurrence of a double-bit memory error since the last reset to the memory error log. If the MER LED is illuminated, all other memory error indicators except the row-in-error information are unreliable.

3.3.3.2 Single-Bit Error. The CER LED indicator designates the occurrence of a single-bit memory error (correctable error) since the last reset to the memory error log. If the CER LED is illuminated, but not the MER LED, then the row-in-error and bit-in-error LEDs pinpoint the memory integrated circuit (IC) causing the error.

NOTE

The 990/10A 1M board does not have ROW or BIT-IN-ERROR LEDs.

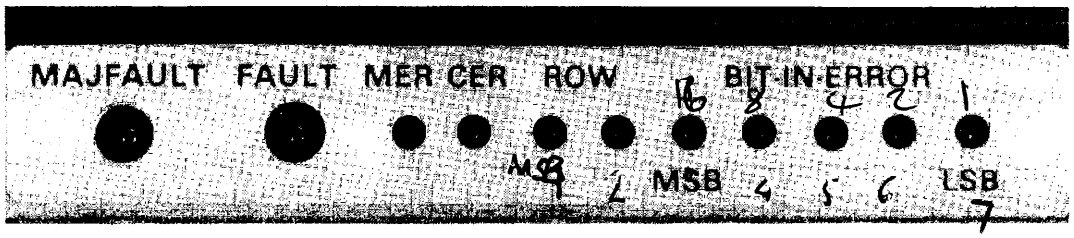

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Figure 3-3. 990/10A Board Failure Indicators

3.3.3.3 ROW. The two ROW LEDs display in binary the logical row of memory chips that contains a single- or double-bit error. The leftmost LED is the most significant binary bit. Decoding and repair of this malfunction should be done only by trained service personnel using properly qualified parts.

3.3.3.4 BIT-IN-ERROR. The five BIT-IN-ERROR LEDs encode in binary the memory IC within the row designated by the ROW LEDs that caused a single-bit memory error.

3.4 990/10A SELF-TEST

The 990/10A has ROM-resident self-test code that exercises the logic on the 990/10A board and indicates the result of the test via the FAULT (or MAJFAULT) LEDs. Self-test, in general, is executed after the 990/10A is powered up (before any other process is performed) and before any load. Two parts of self-test, RAM test and load device verification, are not run every time self-test is executed.

RAM test is run only if it is determined that memory has not been initialized (as is the case on power-up with no standby power) or if an alternate load is being performed.

Load device verification is run as a part of self-test before any load from a TILINE device. Thus, on power-up when a load is not being performed, and on loads from CRU devices, load device verification is not run.

3.4.1 Self-Test Description

The first section of self-test deals with the major fault condition and the remaining sections deal with the logic outside of the major fault data path. A flowchart of the 990/10A self-test code is shown in Figure 3-4.

3.4.1.1 Major Fault Test. The first section of the self-test exercises the microprocessor data path. The microprocessor, the address latch, the loader/self-test ROMs, the scratch pad RAM, the CRU chip, the ready controller, the ready logic, and the oscillator constitute the microprocessor data path. A failure implies that the problem is likely to be a faulty microprocessor chip or loader/self-test ROM. Some of the tests performed in this section are:

- Execute a CRC of the self-test ROMs.
- Test the scatch-pad RAM.
- Execute a representative sample of instructions through the microprocessor and test the results.

If the major fault section of self-test is passed successfully, the major fault LED is extinguished and the remainder of self-test is initiated. If the test is not successful, one (MAJFAULT) or both fault LEDs on the processor board remain illuminated and the processor is inoperative. In case of a MAJFAULT indication, all accesses to on-board or off-board addresses are inhibited.

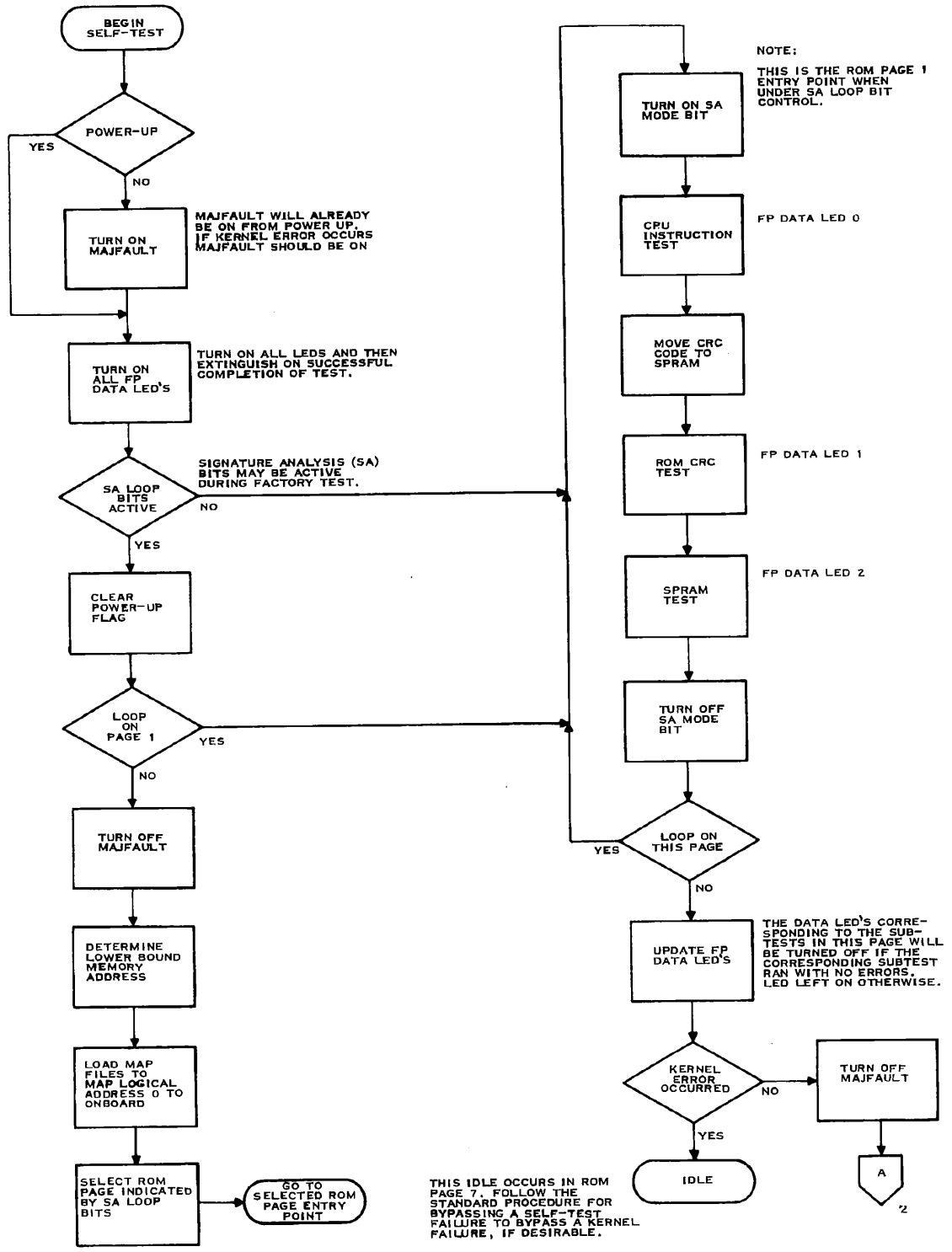

Figure 3-4. Flowchart of 990/10A Self-Test Code (Sheet 1 of 6)

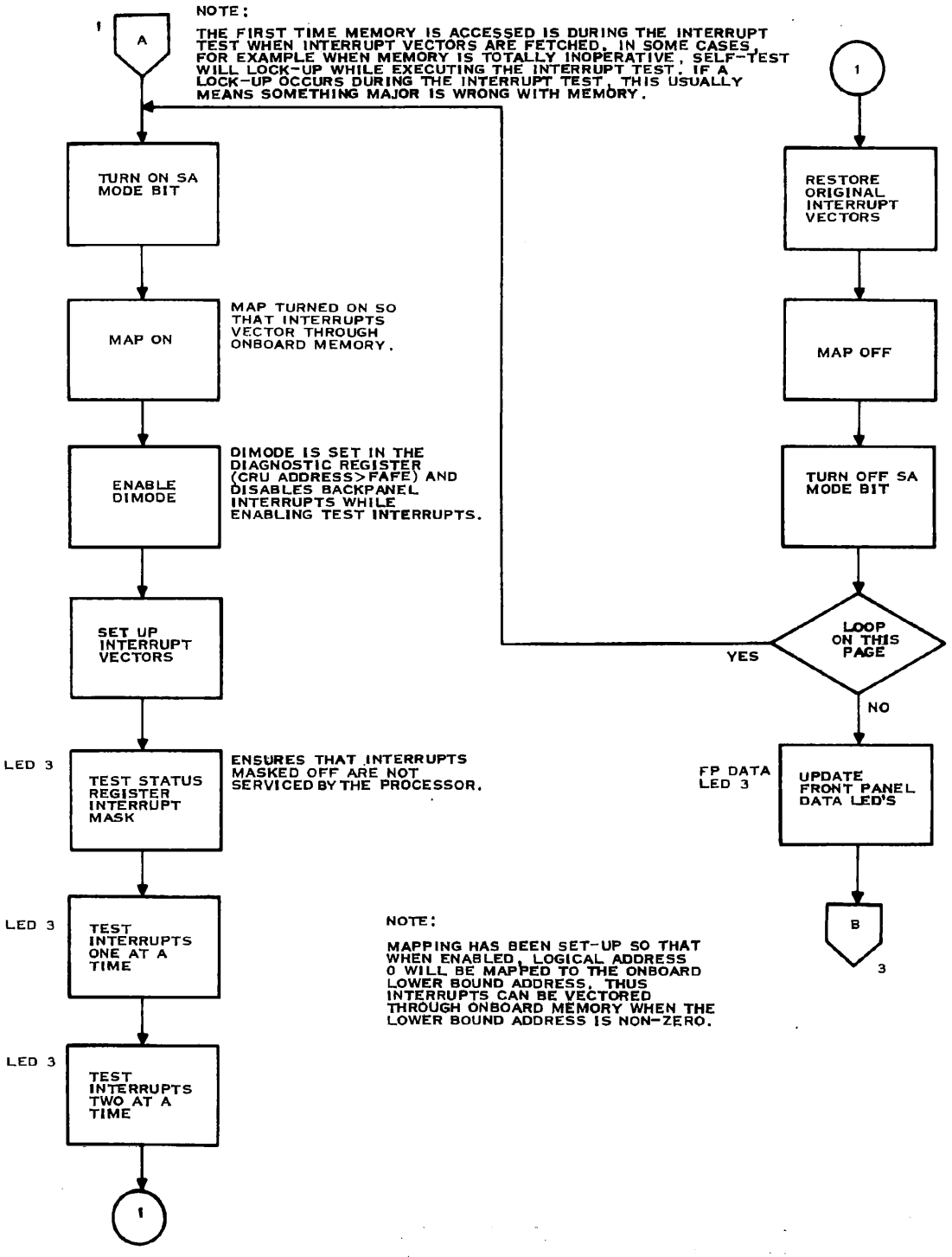

Figure 3-4. Flowchart of 990/10A Self-Test Code (Sheet 2 of 6)

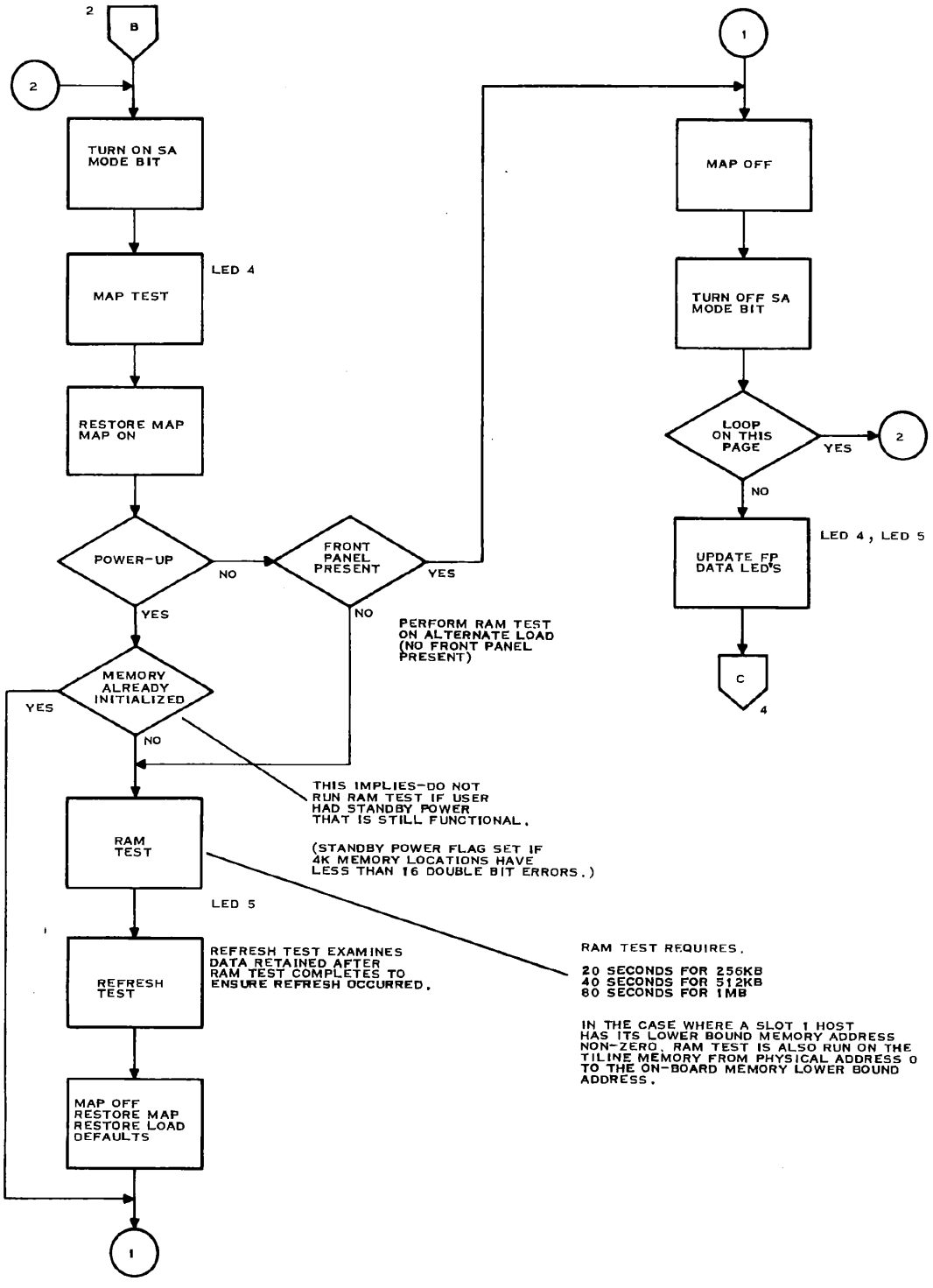

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Figure 3-4. Flowchart of 990/10A Self-Test Code (Sheet 3 of 6)

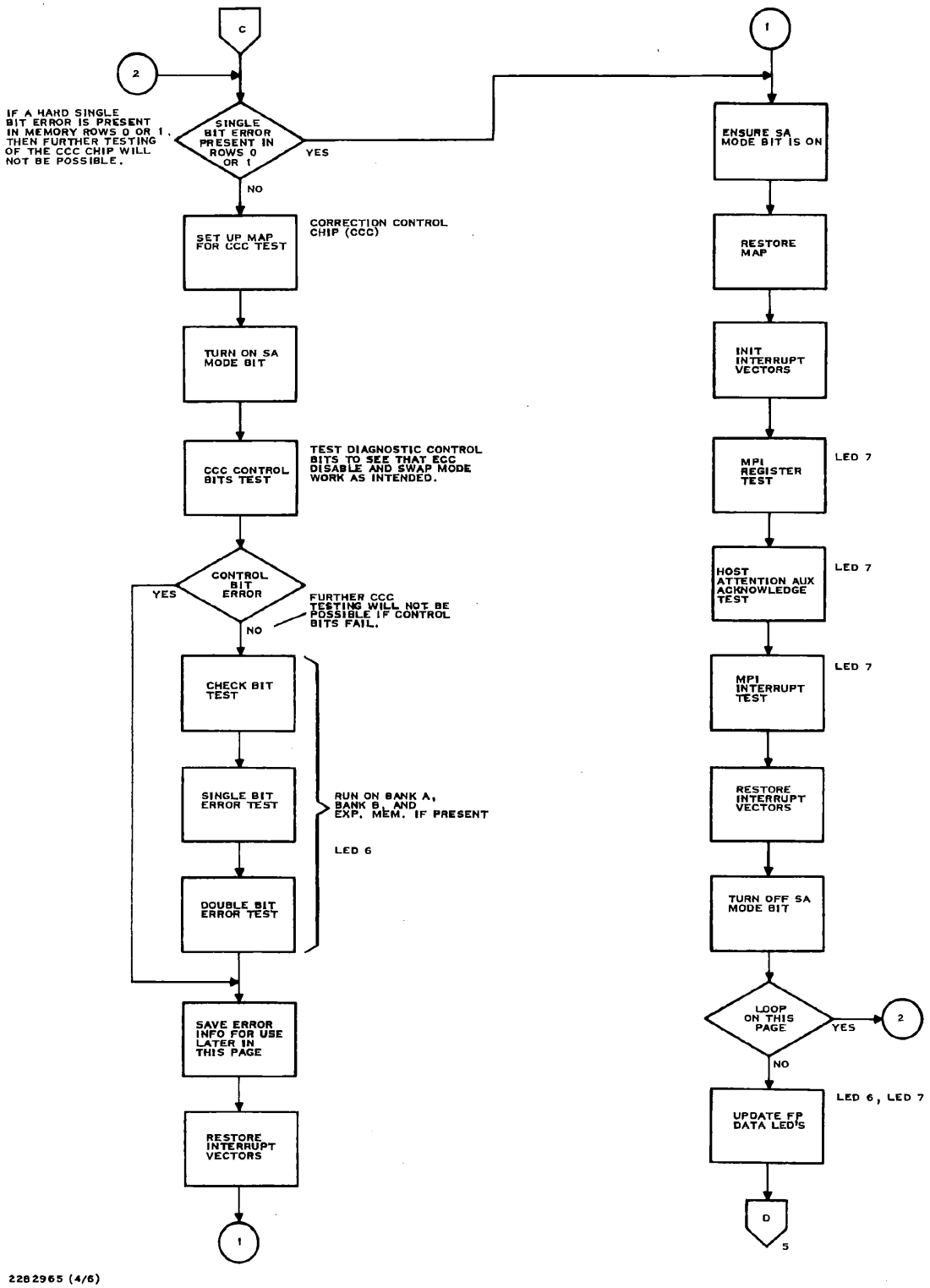

Figure 3-4. Flowchart of 990/10A Self-Test Code (Sheet 4 of 6)

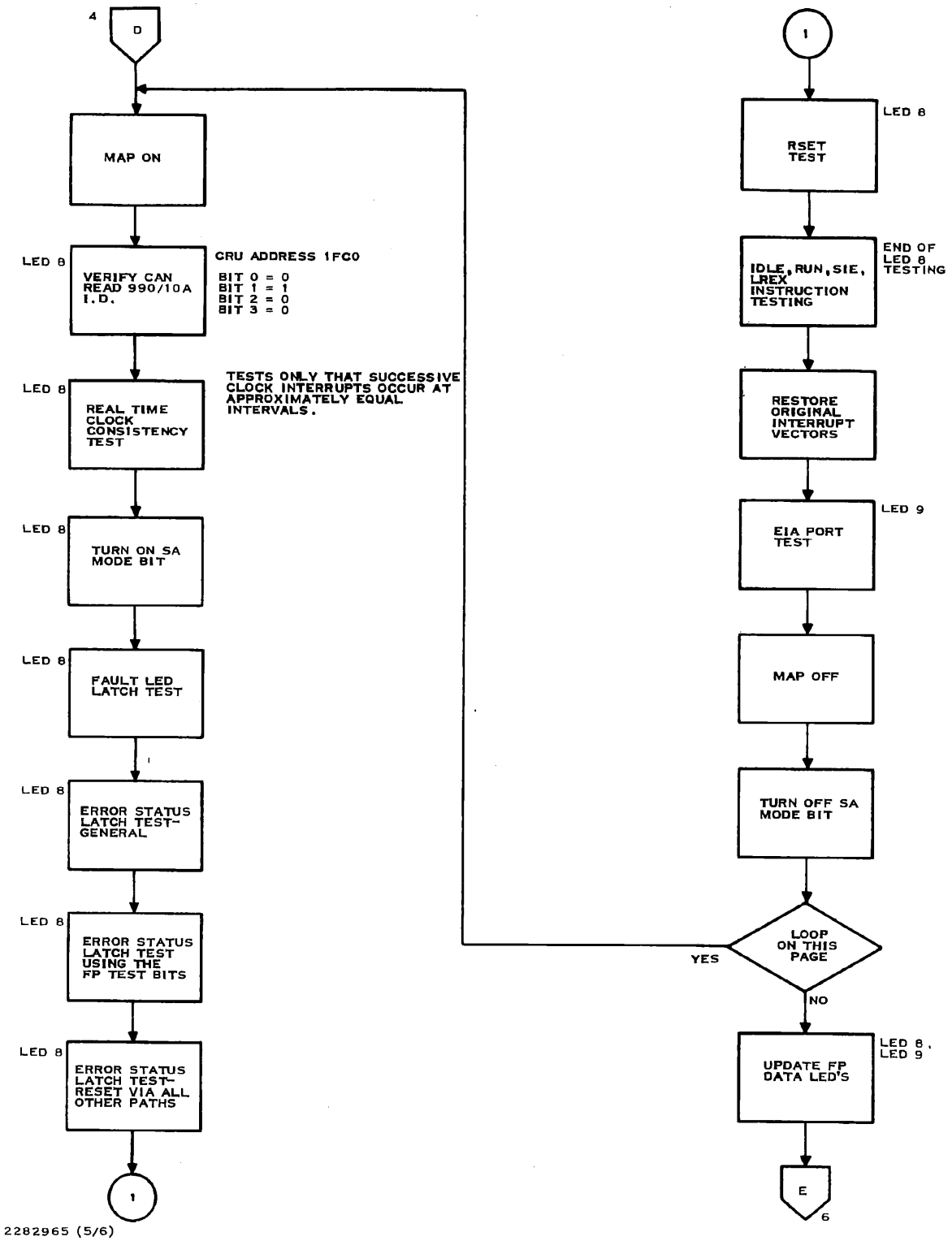

Figure 3-4. Flowchart of 990/10A Self-Test Code (Sheet 5 of 6)

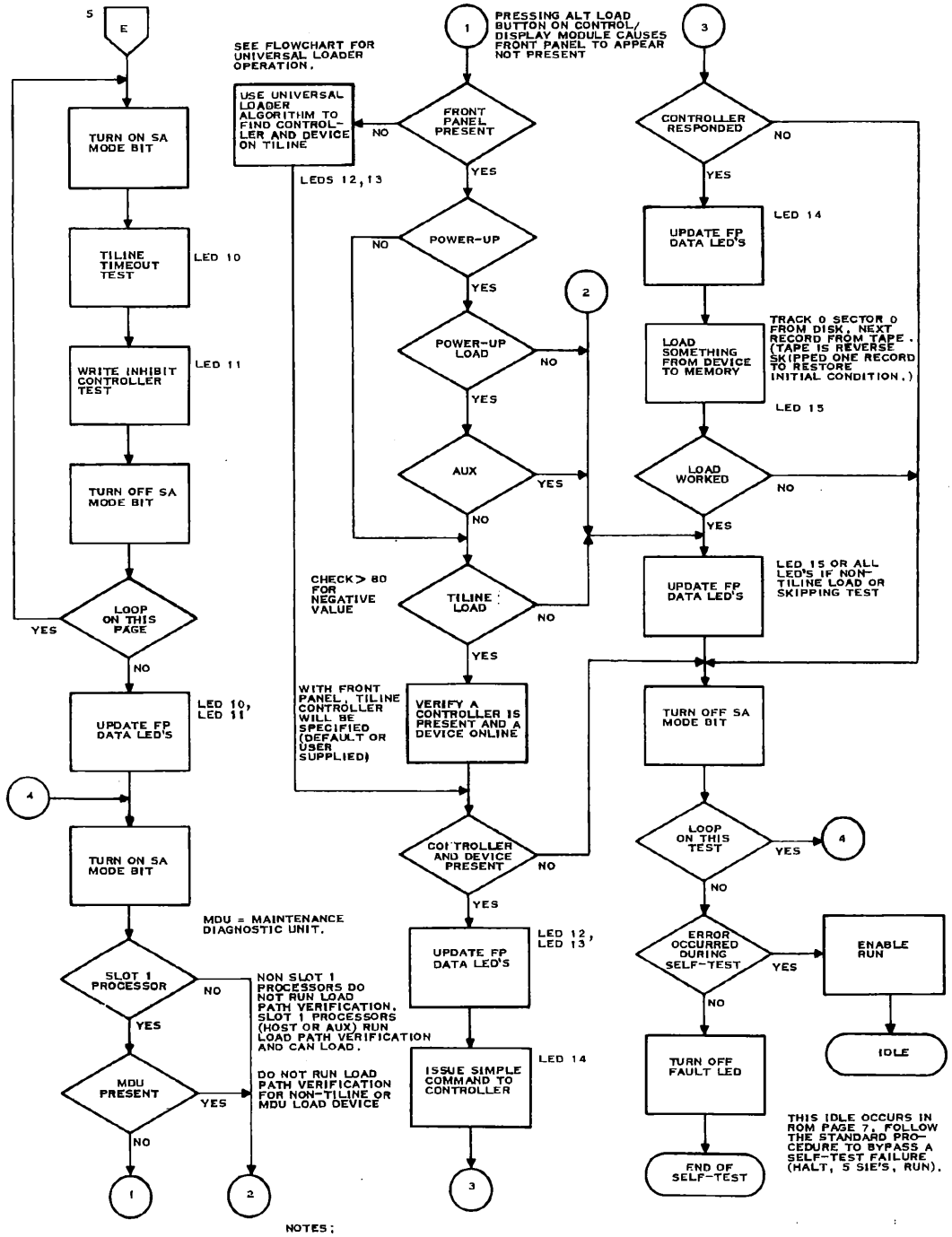

Figure 3-4. Flowchart of 990/10A Self-Test Code (Sheet 6 of 6)

3.4.1.2 General Fault Test. The remaining sections of the self-test exercise major portions of the 990/10A. An overview of the logical sections and their associated tests follows:

- Map chip, address buffer, and address latch check.
  - — Latch and read back mapped addresses to verify all internal registers.
  - — Verify that TPCS address generation is correct.
- RAM test.
  - — Write and read from/to RAM memory with ECC enabled.
  - — Write and read from/to RAM memory with ECC disabled. Reenable ECC and verify that single-bit errors are corrected and double-bit errors detected.
  - — Read the error log to verify that errors were identified.
  - — Verify that 1 and 0 can be written to every bit position in every word in the on-board memory address space. Verify address uniqueness in the on-board address space. This test is not run if battery backup is determined to be present and operational.
- TILINE test.
  - — Initiate loopback test mode to verify operation of external address decode and TILINE slave controller.
  - — Initiate TILINE master cycle to TILINE time-out address (FBFE) and verify that master timed out.
- CRU and interrupt check.
  - — Check interrupts individually and in combinations.
  - — Check CKON, CKOF, LREX, and IDLE external instructions.
  - — Set error status latch, verify interrupt, and clear status individually.
  - — Check front panel logic contained on the central processor.
- Nonload path logic test.
  - — Perform test of multiprocessor logic.
  - — Perform EIA port loopback test.

- Perform load device verification test (runs only before load is attempted).
  - — Verify that a load device is present.
  - — Verify that the load device controller is operational.
  - — Verify that the load device unit is operational.

3.4.2 Self-Test Execution Time

Self-test, excluding RAM test, executes in approximately one second. RAM test requires 20 seconds for 256K bytes, 40 seconds for 512K bytes, and 80 seconds for 1 megabyte to execute. While RAM test is executing, the front panel LEDs alternately display >0F0F and >F0F0.

3.4.3 Self-Test Error Reporting

When self-test execution begins, all error LED's (FAULT and MAJFAULT) are turned on and all F's are displayed on the front panel. As each section of self-test completes, the bit position corresponding to the completed section is changed to 0 if the section completed with no errors. Refer to Figure 3-5 and Table 3-1 for the self-test section to bit position correspondence definition. The only exception to this is while RAM test is executing, the front panel LED's alternately display >0F0F and >F0F0. After completion of RAM test, the front panel display resumes its error information display.

The error LED's are turned off as follows. Major fault (MAJFAULT) is turned off if the first three sections of self-test complete successfully. Should a failure occur in any of these three sections, the 990/10A processor will go to IDLE (if possible) since something major is wrong and further testing is probably not possible. This self-test failure can be bypassed like a self-test fault to force self-test to continue testing. See paragraph 3.4.4 for instructions on how to bypass a self-test failure. If all sections of the general fault test are passed successfully, the FAULT LED will be extinguished and the RUN LED will be illuminated. If the general fault test is unsuccessful, the FAULT LED will be illuminated and the CPU will idle with the IDLE LED on. At this time, the hexadecimal display will display an error code indicating a failure in one or more modules of self-test as defined in Table 3-1. If it is then determined that it is desirable to bypass the failure, refer to paragraph 3.4.4 for instructions on how to bypass a self-test failure.

3.4.4 Bypassing a Self-Test Failure

When a self-test failure occurs, it is possible to bypass the failure and force the processor to continue.

To bypass a self-test failure:

1. Press HALT.
2. Press HALT 5 times.
3. Press RUN.

CAUTION

Do not attempt to execute the loader following a self-test failure without repairing the CPU unless you have a backup copy of the load medium.